IN THE CLAIMS

We claim:

1. A method comprising:

forming a thin film stack on a substrate, wherein the thin film stack includes at least a polysilicon layer and an oxide layer;

forming a hardmask layer on the thin film stack;

forming an anti-reflective coating (ARC) layer on the hardmask layer;

patterning the ARC layer;

etching the hardmask layer using the patterned ARC layer as a mask; and

etching the thin film stack using the hardmask layer as a mask.

2. The method of claim 1, wherein the ARC layer is patterned with resist using 193nm or less lithography.

3. The method of claim 2, wherein the thickness of the resist is less than 5000Å.

4. The method of claim 3, wherein the hardmask layer has a thickness of between 1000 and 3000Å and the ARC layer has a thickness of between 100 and 500Å.

5. The method of claim 3, wherein the hardmask layer comprises a material that has high selectivity to both polysilicon and oxide etch chemistries.

6. The method of claim 3, wherein the hardmask layer comprises amorphous carbon.

7. The method of claim 6, wherein the hardmask layer comprises Applied Materials® Advanced Patterning Film™ (APF™).

8. The method of claim 3, wherein the ARC layer is removed during the etching of the thin film stack.

9. The method of claim 3, further comprising removing the hardmask material from the thin film stack.

10. A method comprising:
forming a flash memory gate stack on a substrate;
forming a hardmask layer on the flash memory gate stack;
forming an anti-reflective coating (ARC) layer on the hardmask layer;
patterning the ARC layer;
etching the hardmask layer using the patterned ARC layer as a mask; and
etching the flash memory gate stack using the hardmask layer as a mask.

11. The method of claim 10, wherein the ARC layer is patterned with resist using 193nm or less lithography.

12. The method of claim 11, wherein the thickness of the resist is less than 5000Å.

13. The method of claim 12, wherein the flash memory gate stack is comprised of a gate dielectric layer, a floating gate layer, an inter-electrode dielectric layer, and a control gate electrode layer.

14. The method of claim 12, wherein the hardmask layer has a thickness of between 1000 and 3000Å and the ARC layer has a thickness of between 100 and 500Å.

15. The method of claim 12, wherein the hardmask layer comprises a material that has high selectivity to both polysilicon and oxide etch chemistries.

16. The method of claim 12, wherein the hardmask layer comprises amorphous carbon.

17. The method of claim 16, wherein the hardmask layer comprises Applied Materials® Advanced Patterning Film™ (APF™).

18. The method of claim 12, wherein the ARC layer is removed during the etching of the flash memory gate stack.

19. The method of claim 12, further comprising removing the hardmask material from the flash memory gate stack.

20. An apparatus comprising:

a substrate;

a thin film stack formed on the substrate, wherein the thin film stack includes at least a polysilicon layer and an oxide layer;

a carbon-based layer formed on the thin film stack; and

an anti-reflective coating (ARC) layer formed on the carbon-based layer.

21. The apparatus of claim 20, wherein the carbon-based layer has a thickness of between 1000 and 3000Å and the ARC layer has a thickness of between 100 and 500Å.

22. The apparatus of claim 20, wherein the carbon-based layer comprises a material that has high selectivity to both polysilicon and oxide etch chemistries.

23. The apparatus of claim 22, wherein the carbon-based layer comprises amorphous carbon.

24. The apparatus of claim 23, wherein the carbon-based layer comprises Applied Materials® Advanced Patterning Film™ (APF™).

25. The apparatus of claim 20, wherein the ARC layer comprises silicon dioxide, silicon oxynitride or a composite thereof.

26. An apparatus comprising:

a substrate;

a thin film stack formed on the substrate, the thin film stack having a top surface, wherein the thin film stack includes at least a polysilicon layer and an oxide layer;

a first layer formed on the top surface of the thin film stack, wherein the first layer comprises a material that will not erode during either a polysilicon etch process or an oxide etch process; and

a second layer formed on the first layer, wherein the second layer comprises a material which reduces undesirable light reflections and which may erode during either a polysilicon etch process or an oxide etch process.

27. The apparatus of claim 26, wherein the first layer has a thickness of between 1000 and 3000Å and the second layer has a thickness of between 100 and 500Å.

28. The apparatus of claim 26, wherein the first layer comprises amorphous carbon.

29. The apparatus of claim 28, wherein the first layer comprises Applied Materials® Advanced Patterning Film™ (APF™).

30. The apparatus of claim 26, wherein the second layer comprises silicon dioxide, silicon oxynitride or a composite thereof.